Mini-Circuits®

IMPROVED ERA AMPLIFIERS
(AN-60-010)

Introduction

The improved Mini-Circuits ERA series of amplifiers offer the RF designer multi-stage performance in a package which looks like a discrete transistor. Improved ERA amplifiers' advantages of wide bandwidth, impedance match, and a choice of gain and output power levels result from their being monolithic circuits which contain InGaP HBTs (indium gallium phosphide heterojunction bipolar transistors).

Applying DC power to operate an Improved ERA is simpler than biasing a transistor. This article gives the user step-by-step guidance in choosing external bias circuit components to obtain optimum performance.

The internal circuit configuration is a Darlington pair, embedded in a resistor network as shown in the schematic diagrams, Figure 1. Like a discrete bipolar transistor, this type of circuit is current- rather than voltage-controlled. This means that for a range of current around a recommended value, the device voltage varies much less than in proportion to current. A constant-current DC source would be ideal for providing a stable operating point. By contrast, if a constant-voltage DC source were used the current would vary widely with small changes in supply voltage, temperature change, and device-to-device variations; such operation is not recommended. Practical applications typically use a series resistor between the Improved ERA and a source of DC voltage to approximate constant current; so, how best to use this technique is a one of the themes of this article.

An Improved ERA amplifier is a 2-port device: RF input, and combined RF output and bias input. It has 4 leads including 2 ground leads; connecting both of them to external ground will minimize common path impedance for best RF performance. Internal resistors in Figure 1 determine the DC operating point of the transistors and provide feedback to set RF gain, bandwidth, and input and output impedances to optimum values.

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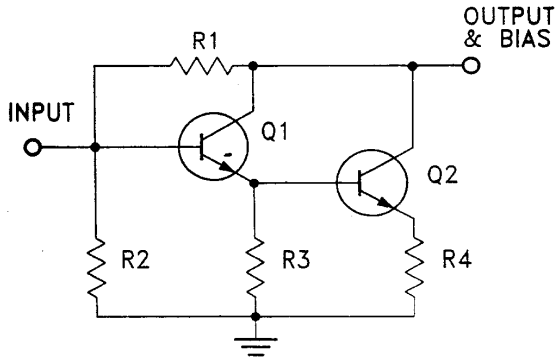
Figure 1 Schematic Diagram



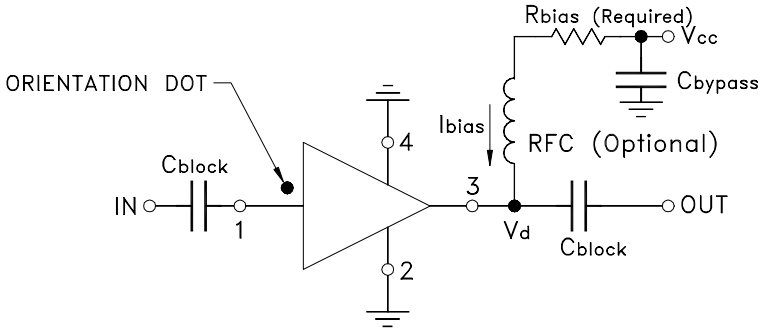
Bias Circuit

A practical biasing configuration is shown in Figure 2. Bias current is delivered from a voltage supply V_{cc} through the resistor R_{bias} and the RF choke (inductor), shown as RFC in the figure. The resistor reduces the effect of device voltage (V_c) variation on the bias current by approximating a current source.

Blocking capacitors are needed at the input and output ports. They should be of a type having low ESR (effective series resistance), and should have reactance low enough not to affect insertion loss or VSWR adversely at low frequency. The blocking capacitors must be free of parasitic resonance up to the highest operating frequency. Use of a bypass capacitor at the connection to the DC supply is advised to prevent stray coupling to other signal processing components.

Figure 2 Typical biasing Configuration for Improved ERA Amplifiers

In this circuit, DC blocking capacitors are added at the input port (pin number 1 on the packaged amplifier) and at the output port (pin 3).



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Bias current is given by the equation:

$$I_{bias} = (V_{cc} - V_d) \div R_{bias}$$

Table 1 lists the values of the bias resistor needed with several values of supply voltage for each of the Improved ERA models. These values take into account the variation of device voltage, both lot-to-lot and with temperature (-45 to 85°C ambient). Also, they are chosen from the readily available "1%" resistor values. The table lists the power dissipated by the bias resistor in the 12-volt case, as an example. The greater the difference between the supply and device voltage, the easier it is to maintain constant operating conditions; this is discussed in detail later.

The bias current values in Table 1 are the recommended values. The effect on RF performance and MTTF of using different currents is discussed later in this Application Note. Exceeding the maximum current values shown there, however, could cause excessive junction temperature and premature failure. Substantially lower currents, while not degrading device reliability, could cause unpredictable RF performance because of non-optimum internal operating points.

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Table 1 Bias Resistor Values for Various Supply Voltages

Improved ERA Model	ERA-1	ERA-2	ERA-21	ERA-3	ERA-33	ERA-4	ERA-50	ERA-51	ERA-6
Bias Current	40 mA	40 mA	40 mA	35 mA	40 mA	65 mA	60 mA	65 mA	70 mA
Device Voltage (nom.)	3.4V	3.5V	3.5V	3.2V	4.3V	4.5V	4.4V	4.5V	4.9V
Supply Voltage	Bias Resistor (ohms) at Supply Voltage								
7	90.9	88.7	88.7	107	69.8	38.3	47.5	40.2	30.1
8	113	113	113	133	93.1	52.3	63.4	53.6	43.2
9	137	137	137	162	115	66.5	78.7	68.1	56.2
10	162	162	162	191	140	80.6	95.3	82.5	69.8
11	187	187	187	221	165	95.3	113	97.6	84.5
12	215	215	210	249	191	110	127	113	97.6
13	237	237	237	280	215	127	143	127	113
14	261	261	261	309	243	143	162	143	127
15	287	287	287	340	267	158	178	158	140
16	309	316	316	365	287	174	196	174	154
17	332	340	340	392	316	187	210	191	169
18	357	365	365	422	340	205	226	205	182
19	383	392	392	453	365	221	243	221	196
20	412	412	412	475	392	237	261	237	210
Nominal dissip. in Resistor for 12V	0.34 W	0.34 W	0.34 W	0.31 W	0.31 W	0.51 W	0.45 W	0.50 W	0.52 W

Advantage of an RF Choke

The advisability of using an RF choke in series with R_{bias} is evident from the following analysis. Figure 3 shows an equivalent circuit of the output of an Improved ERA amplifier as a current source in parallel with an internal 50-ohm source resistance, loaded by both R_{bias} and an external 50-ohm load. The current in the 50-ohm load is:

$$I_{source} \times R_{bias} \div (2\ R_{bias} + 50)$$

and the loss in power gain relative to not having the output loaded by R_{bias} is:

$$20 \log [(2\ R_{bias} + 50) \div 2\ R_{bias}]\ \text{dB}.$$

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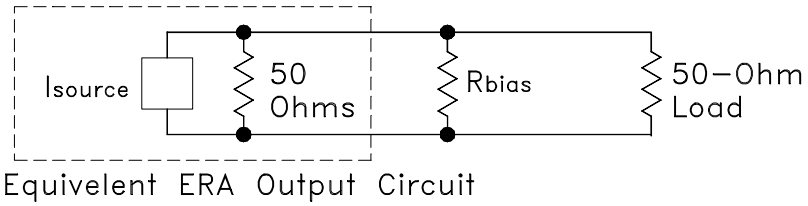
Figure 3 Effect of Bias Resistor on the Output, Without an RF Choke



Suppose, for example, that the Improved ERA-4 is used with a 12-volt supply without a choke. From the above expression, the effect of the 114-ohm bias resistor (from Table 1) is found to be a 1.7 dB reduction in the gain of the amplifier.

An RF choke should be chosen such that its reactance is at least 500 ohms (10 times the load impedance) at the lowest operating frequency. It must also be free of parasitic (series) resonance up to the highest operating frequency.

Super Wide-band RF Choke

The circuit designer might consider using a commercially available inductor as the RF choke in the bias circuit of Figure 2. The low end of the useful frequency range is controlled by the value of the inductance; the higher the value, the lower the frequency. The high end of the frequency range is determined by the series resonant frequency of the inductor; it tends to decrease as the value of the inductance increases. The frequency band of the overall amplifier circuit is often limited by the inductor rather than the Improved ERA devices, which have performance up to 8 GHz. Besides, inductors are not clearly specified for RF choke application, and design change by the inductor manufacturer will have an unknown effect on the circuit. This complicates the circuit designer's job.

Mini-Circuits solves the problem by offering a super wide-band RF choke covering 50 to 8000 MHz, which enables circuit designers to utilize easily the full capability of the Improved ERA series. The RF choke is 2-terminal device in a 0.31 by 0.22-inch surface mount package available with 2 pin-outs, designated as models ADCH-80 and ADCH-80A, to accommodate different PC board layouts.

The equivalent inductance of the Super Wide-band RF choke is one microhenry at 100 mA. For comparison, a typical commercially available one-microhenry inductor has a series resonant frequency as low as 90 MHz, which is much lower than this RF choke. Figure 4 plots the insertion loss and Figure 5 the VSWR at various currents up to 100 mA, for the RF choke placed in shunt across a 50-ohm transmission line. Note that the insertion loss and VSWR change very little with change in current in the specified frequency band.

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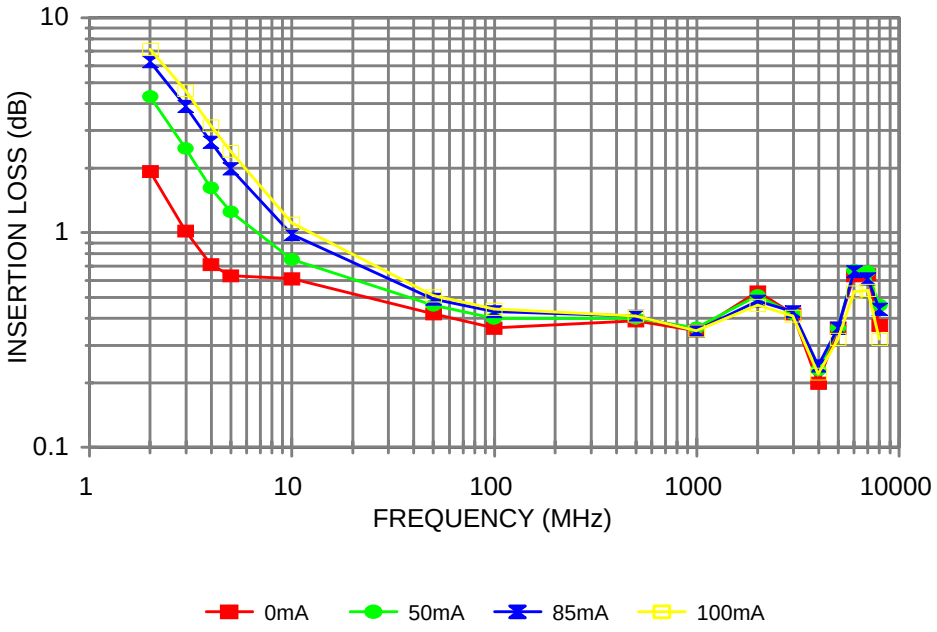

Figure 4 Insertion Loss of the RF Choke

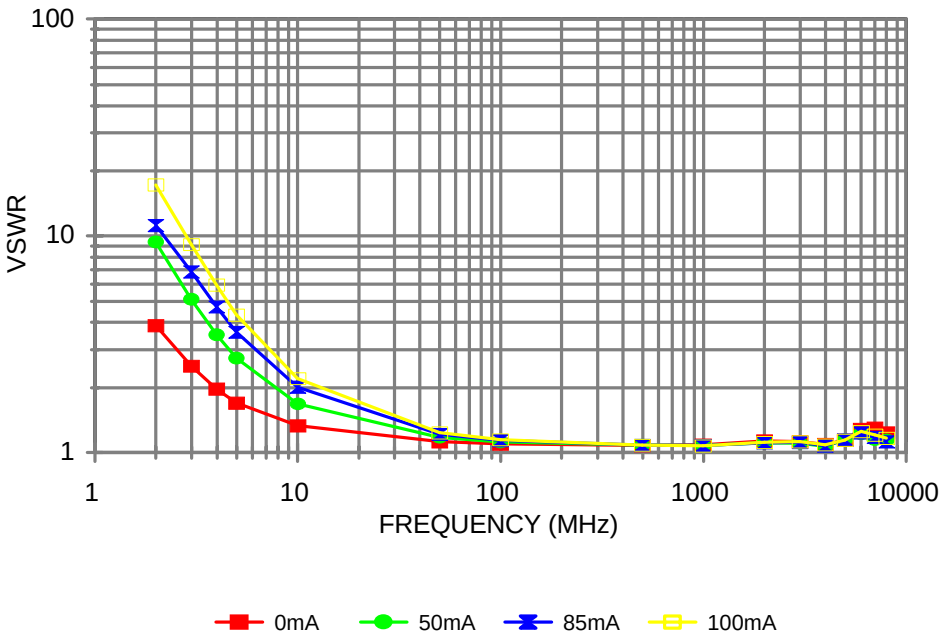

Figure 5 VSWR of the RF Choke

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Higher Bias Resistor Values Reduce Variation

Increasing the supply voltage allows a higher value of R_{bias} to be used as shown in Table 1, and that reduces the variation in bias current. The benefit is that RF performance, especially the 1-dB compression point, is made more constant. The following quantifies this effect.

The device voltage V_d is a function of both I_{bias} and temperature T. Device voltage increases with bias current, and the variation can be expressed as a rate of change

$$\Delta V_d / \Delta I_{bias},$$

in mV per mA. Device voltage decreases with increasing temperature, as

$$\Delta V_d / \Delta T$$

millivolts per degree C. Typical values for these variation coefficients are listed in Table 2 for the Improved ERA devices.

Table 2 Improved ERA Device Voltage Variation with Current and Temperature

Improved ERA Model No.	Nominal Bias Current, mA	Typ. Device Voltage Variation with Current, $\Delta V_d/\Delta I_{bias}$ (mV/mA)	Typ. Device Voltage Variation with Temperature, $\Delta V_d/\Delta T$ (mV/°C)
ERA-1	40	8.0	- 2.4
ERA-2	40	6.0	-2.5
ERA-21	40	8.7	-2.4
ERA-3	35	3.3	-2.4
ERA-33	40	6.0	-3.5
ERA-4	65	9.3	-2.9
ERA-50	60	5.8	-3.4
ERA-51	65	5.6	-3.2
ERA-6	70	14.0	-3.1

The combined effect of the two device-voltage coefficients can be expressed as variation of bias current with temperature, derived as follows:

$$I_{bias} = [V_{cc} - V_d(I_{bias}, T)] \div R_{bias},$$

where $V_d(I_{bias}, T) = V_0 + (\Delta V_d / \Delta I_{bias}) \cdot I_{bias} + (\Delta V_d / \Delta T) \cdot (T - T_0)$

The "Δ" ratios are the coefficients from Table 2. V_0 is the V_d-axis intercept of the linear V_d vs. I_{bias} curve, at room temperature T_0. Substituting for V_d and solving for I_{bias}:

$$I_{bias} = [V_{cc} - V_0 - (\Delta V_d / \Delta T) \cdot (T - T_0)] \div [R_{bias} + (\Delta V_d / \Delta I_{bias})]$$

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Differentiating with respect to T gives the desired result:

$$\Delta I_{bias} / \Delta T = -(\Delta V_d / \Delta T) \div [R_{bias} + (\Delta V_d / \Delta I_{bias})]$$

To find the change in bias current that will typically occur with a given change in temperature ΔT, substitute values for the device-voltage coefficients from Table 2, and the value of bias resistor being considered, into the right-hand side of the equation. Multiplying the result by ΔT yields the change in bias current ΔI_{bias}.

To illustrate the effect of supply voltage, let us consider two examples for the Improved ERA-1, based upon Tables 1 and 2. For V_{cc} = 5 volts and R_{bias} = 40 ohms,

$$\Delta I_{bias} / \Delta T = -(-2.4) \div (40 + 8) = .050 \text{ mA/°C}.$$

Over an operating temperature range of −45 to 85 degrees C, the total variation in current for this example will be 6.5 mA, which is more than 15% of the recommended value of current. The consequence is about 1.6 dB variation in output power at 1-dB compression.

For the second example, try V_{cc} = 12 volts and R_{bias} = 215 ohms. A similar calculation yields 1.4 mA total variation in current, which causes less than 0.5 dB variation in output power.

Additional Sources of Variation

The variation of device voltage as discussed above pertains to an individual device. The specifications include the limits of device voltage that the various Improved ERA models must meet. Actual expected unit-to-unit variation is much less than indicated by those limits, because of the high degree of process control used during manufacture. Therefore, a user can be confident that results obtained when prototyping products that incorporate Improved ERA that performance will be highly repeatable.

Besides the variation of bias current due to the characteristics of the Improved ERA itself, there are two additional causes that the user might need to consider:

- Available nominal values, tolerance and temperature coefficient of the bias resistor.
- Voltage setting error and regulation of the power supply.

Resistors readily available are generally the “1% values”. The nominal values, having increments of 2%, could thus differ from the Table 1 values by as much as ±1%. If a resistor having temperature coefficient of 200 ppm/°C is used, it could vary ±1.5% over the −45 to 85°C range. The resistance, and correspondingly the bias current,

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might therefore be as much as 2.5% different from the desired value in Table 1 due to these contributions.

Good DC power supplies typically have about 10 mV combined line and load regulation, and that tends not to be an important factor. However, the tolerance of a fixed-voltage supply, or setting accuracy of a field adjustable one might be ±1%. As an example, consider the Improved ERA-51 being used with a 9-volt supply. Since the nominal device voltage is 4.5 V (half the supply voltage), a 1%, error in supply voltage would change the current by 0.5%.

The combination of the resistor and power supply variations in the above example would cause 2.5% + 0.5% = 3% error in current, which is 2 mA for a nominal value of 65 mA. Besides, the temperature effect on current in the Improved ERA-51 device itself, using the formula under Table 2, is:

$$\Delta I_{bias} / \Delta T = -(-3.2) \div (69 + 6.7) = .042 \text{ mA/°C.}$$

Relative to the room temperature value, current would change ±3 mA with temperature. The overall combined variation, including the bias resistor and power supply effects, is ±5 mA for this example. A user working within an MTTF or current consumption budget who needs to ensure that 65 mA is not exceeded may therefore choose to design for a nominal value of 60 mA in this example.

Minimizing Power Dissipation

In addition to bias current stability, stability of power dissipation of the Improved ERA device is favored by using a high V_{cc} value. This is because of the negative temperature coefficient of device voltage V_d. In particular, if V_{cc} is at least 2 times V_d, then P_D, the Improved ERA power dissipation decreases with increasing temperature, as shown by the following analysis:

$$P_D = V_d \cdot I_{bias} = V_d (V_{cc} - V_d) \div R_{bias}$$

Taking the derivative of P_D with respect to V_d and setting it equal to zero, we find that the maximum value of P_D occurs when $V_d = V_{cc} \div 2$. This is illustrated in Figure 6.

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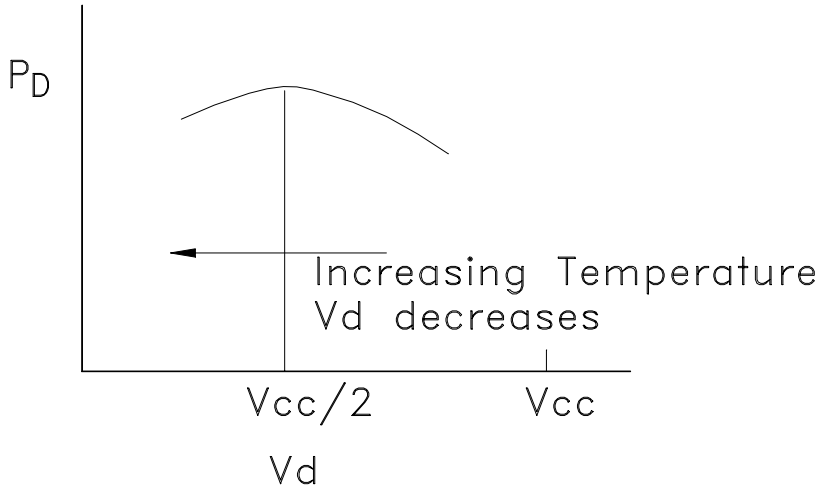
Figure 6 Variation of Improved ERA Power Dissipation with Temperature, for Device Voltage Above, and Below, Half the Supply Voltage Value



Let us see what happens to power dissipation in the case of Improved ERA-4 between 25 and 85 degrees C, for two values of supply voltage: one less than, and another greater than, twice the value of V_d. We will use 65 mA and 4.5 V as the nominal (room temperature) values of I_{bias} and V_d.

To find the change in P_D, the power dissipation of the Improved ERA amplifier, we must use the equations for I_{bias} and V_d with which we started, above, in order to account for the interdependence of these quantities as well as temperature.

$I_{bias} = [V_{cc} - V_0 - (\Delta V_d / \Delta T) \cdot (T - T_0)] \div [R_{bias} + (\Delta V_d / \Delta I_{bias})]$, as before.

Substituting for I_{bias} in the V_d equation and solving for V_d:

$$V_d = [R_{bias} \cdot V_0 + (\Delta V_d / \Delta I_{bias}) \cdot V_{cc} + R_{bias} \cdot (\Delta V_d / \Delta T) \cdot (T - T_0)] \div [R_{bias} + (\Delta V_d / \Delta I_{bias})]$$

P_D can now obtained as the product of right-hand sides of these two equations. The constant V_0 is found by subtracting $[I_{bias} \times (\Delta V_d / \Delta I_{bias})]$ from V_d, using the room-temperature values of I_{bias} and V_d.

For V_{cc} = 5.0 V, R_{bias} = 7.7 ohms. Using the value −2.9mV/°C for the V_d temperature coefficient from Table 3 and the above equations, P_D increases from .293 watt at 25°C to .331 watt at 85°C. Considering the thermal resistance of Improved ERA-4 (junction-to-case) of 177°C/W, this increase in power dissipation results in 7°C higher junction temperature than if dissipation were constant. The consequence in reliability is a factor of 2 reduction in MTTF.

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Now, try V_{cc} = 12 V, for which R_{bias} = 115.4 ohms. For this case, P_D decreases from .293watt at 25°C to .288 watt at 85°C.

Temperature Compensated Bias Network

An alternative method of biasing the Improved ERA which allows use of lower supply voltage while maintaining bias current stability and reducing power dissipation in the bias resistor is to use a temperature compensating bias network in place of the single resistor R_{bias}. The network consists of a linear positive-temperature-coefficient chip thermistor in parallel with a regular chip resistor, and should be designed so that its resistance increases with temperature just enough to make up for the decrease in device voltage, causing the Improved ERA current to remain constant.

Commercially available chip thermistors have a very high TCR (temperature coefficient of resistance), typically +4500 ppm/°C for the range 51 - 510 ohms. The temperature coefficient needed for R_{bias} is much less than this, and thus achievable by using the 2-components (resistor and thermistor) in parallel.

We now derive the values of the network components. Let R be the resistance of the regular resistor, and R_t the 25°C resistance of the thermistor.

Let k_b be the fractional increase in R_{bias} needed at the maximum operating temperature relative to 25°C: (hot resistance − 25°C resistance) ÷ 25°C resistance.

Let k_t be the fractional increase in resistance of the thermistor,
$(4500 \times 10^{-6}) \times$ (maximum operating temperature − 25°C).

Because the resistor and thermistor are in parallel they must satisfy:

$R_{bias} = R \cdot R_t \div (R + R_t)$ at 25°C, and
$(1 + k_b)\, R_{bias} = R \cdot R_t\, (1 + k_t) \div [R + R_t\, (1 + k_t)]$
at the maximum operating temperature.

Solving these equations yields:

$R = R_{bias} \cdot k_t\, (1 + k_b) \div (k_t - k_b)$, and $R_t = R_{bias} \cdot k_t\, (1 + k_b) \div [k_b\, (1 + k_t)]$

Let us compare simple resistor biasing with the temperature compensating network for biasing an Improved ERA-6 with a 7.0 V supply. Let I_{bias} = 70 mA and V_d = 4.9 V (at 25°C), and use the R_{bias} value 30.1 ohms from Table 1. If we use an ordinary resistor

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for R_{bias} without a thermistor, the current will increase to 74 mA.

Now, we compute the network component values needed to make the current 70 mA at 85°C as well as at 25°C. At 85°C, $V_d = 4.9 - (.0031 \text{ V/ °C}) \times (60°C) = 4.71V$, and R_{bias} should become 32.7 ohms. Thus, $k_b = (32.7 - 30.1) \div 30.1 = .0864$. Also, $k_t = (4500 \times 10^{-6}) \times (85° - 25°) = .27$. Applying the formulas,

$R = 30.1 \times .27 (1 + .0864) \div (.27 - .0864) = 48.1$ ohms

$R_t = 30.1 \times .27 (1 + .0864) \div [.0864 (1 + .27)] = 80.5$ ohms

If the thermistors are available only in "5% values", sufficiently close compensation is obtained by using R_t = 82 ohms and R = 47.5 ohms (for 30.1-ohm parallel equivalent).

For different supply voltages and device operating points different resistor and thermistor values are needed, but the same concept and method can be used. The benefit is the ability to keep the device current constant over temperature, thereby avoiding increase in power dissipated in the amplifier and reduction in MTTF.

We have not mentioned the resistance-temperature coefficient of the ordinary resistor in the bias network. The reason is that thick film chip resistors typically have a coefficient of ±100 ppm/°C. This is about 2% of the TCR of the thermistor, and does not influence the results significantly. A word of caution is due regarding the thermistor, however. Its temperature characteristic is controlled only at 25°C and at 75°C. The user should test actual circuit operation at other temperatures of interest.

RF Performance vs. Device Current

Performance characteristics of Improved ERA devices have been evaluated at several values of bias current, to show users what trade-off they may expect against power consumption. The testing was done at room (25°C) ambient. Results are summarized in Table 3. Entries for the recommended values of current are shown in bold type.

The most pronounced effect of changing the current is in output power at 1-dB compression, and third-order intercept point (IP_3). For Improved ERA-1 as an example, decreasing the current 5 mA from the recommended value decreases the output by 1.6 dB, and increasing it 10 mA increases the output by 2.0 dB. The other models show the same amount or somewhat less increase in output when used at higher current. Taking an average of the four higher power models, decreasing the current 10 mA from the recommended value decreases the output by about 1.5 dB; increasing it

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10 mA increases the output by about 1 dB. The accompanying graphs show output power at 1-dB compression vs. frequency, with current as a parameter. IP_3 essentially tracks these dB changes.

Gain increases only slightly with increasing current: 0.09 dB per 5 mA for -1, -2, and -21 models, and 0.19 and 0.13 dB per 5 mA for the -3 and -33 models respectively. The three highest power models (-4, -51, and –6) change only about 0.04 dB per 5 mA.

Less change occurs in the other characteristics – flatness, VSWR, and noise figure – and in most cases it is insignificant for practical application.

RF Performance vs. Temperature

We also evaluated performance characteristics over the entire operating temperature range, −45 to 85°C, at the current recommended in the specifications for each model. Improved ERA-6 was tested at both 65 mA and 70 mA. The results are shown in the last set of graphs.

At low frequency, data from which the graphs were plotted show that gain of Improved ERA-33 increases with temperature by 0.23 dB from −45 to 85°C, with slope of +0.0018/°C. Data on all of the other models show 0.12 dB or less variation, and in most cases gain is maximum around room temperature. At frequencies above 1 GHz the curves gradually separate, gain decreasing with increasing temperature. Typically there is less than 2dB of variation with temperature at 8 GHz.

Output power at 1-dB compression shows very little change with temperature up to 1 or 2 GHz. It decreases with increasing temperature at higher frequencies. At 4 GHz for example, the graphs show that the change ranges from ±0.5 dB for Improved ERA-1 to ±1.1 dB for Improved ERA-3, at −45 and 85°C relative to 25°C. Third-order intercept point (IP_3) also generally decreases with increasing temperature. For the lower power models the graphs show IP_3 test results at 2 GHz; for the higher power models the test frequency is 1 GHz. The temperature effect ranges from ±0.5 dB (for Improved ERA-33) up to about ±2 dB.

Noise figure decreases with increasing temperature. The effect is fairly uniform over the frequency range up to about 4 GHz, with the curves diverging a little to 8 GHz. There is not much difference in noise figure vs. temperature among the models. At 2 GHz for example, total variation over −45 to 85°C ranges from 0.9 to 1.1 dB.

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Table 3 Typical Improved ERA Performance at Various Bias Currents

Improved ERA Model No.	Device Current mA	Gain @2GHz dB	Flatness to 2GHz ±dB	VSWR IN @2GHz	VSWR OUT @2GHz	IP3 @2GHz dBm	Noise Figure, dB @2GHz	Pout , dBm @1dB Comp. 2GHz
ERA-1	35	11.85	0.43	1.43	1.43	25.4	4.5	10.3
	40	**11.99**	**0.44**	**1.46**	**1.46**	**27.9**	**4.4**	**11.9**
	45	12.06	0.44	1.48	1.47	29.0	4.4	13.2
	50	12.11	0.45	1.49	1.48	29.0	4.5	13.9
ERA-2	35	15.14	0.63	1.45	1.06	26.8	4.0	12.1
	40	**15.26**	**0.63**	**1.46**	**1.08**	**28.3**	**4.0**	**13.3**
	45	15.34	0.64	1.46	1.09	28.7	4.0	13.5
	50	15.40	0.65	1.46	1.11	28.6	4.0	13.7
ERA-21	35	13.15	0.60	1.11	1.33	26.3	4.0	11.0
	40	**13.27**	**0.63**	**1.12**	**1.32**	**28.3**	**4.0**	**12.6**
	45	13.35	0.63	1.14	1.33	29.8	4.0	13.6
	50	13.43	0.63	1.15	1.34	30.4	4.1	14.3
ERA-3	25	18.87	1.74	1.68	1.13	23.0	3.2	9.3
	30	19.13	1.83	1.68	1.16	24.8	3.2	11.2
	35	**19.26**	**1.91**	**1.69**	**1.17**	**25.8**	**3.2**	**12.5**
	40	19.40	1.96	1.69	1.21	26.2	3.2	13.1
ERA-33	35	17.29	0.87	1.82	1.22	27.7	3.9	12.1
	40	**17.45**	**0.89**	**1.81**	**1.19**	**29.9**	**3.9**	**13.8**
	45	17.52	0.93	1.80	1.17	30.8	3.9	15.0
	50	17.68	0.91	1.76	1.16	30.7	4.0	15.8
Improved ERA Model No.	**Device Current mA**	**Gain @1GHz dB**	**Flatness to 2GHz ±dB**	**VSWR IN @1GHz**	**VSWR OUT @1GHz**	**IP3 @1GHz dBm**	**Noise Figure, dB @1GHz**	**Pout , dBm @1dB Comp. 1GHz**
ERA-4	55	14.04	0.44	1.20	1.20	32.5	3.8	16.1
	65	**14.13**	**0.45**	**1.25**	**1.20**	**34.2**	**3.9**	**17.4**
	70	14.17	0.44	1.22	1.20	34.8	3.9	17.9
	80	14.22	0.44	1.23	1.20	34.7	4.0	18.5
ERA-50	50	19.05	1.7	1.36	1.13	31.1	3.1	15.3
	55	19.13	1.7	1.37	1.15	32.6	3.1	16.3
	60	**19.22**	**1.8**	**1.38**	**1.16**	**34.4**	**3.1**	**17.2**
	65	19.30	1.8	1.39	1.17	35.6	3.1	17.8
ERA-51	55	17.33	0.84	1.09	1.28	33.6	3.3	16.6
	65	**17.45**	**0.86**	**1.08**	**1.26**	**36.6**	**3.4**	**18.1**
	70	17.49	0.87	1.09	1.25	37.8	3.4	18.4
	80	17.56	0.87	1.09	1.25	37.8	3.5	19.0
ERA-6	55	12.57	0.23	1.16	1.40	33.3	4.2	16.2
	65	12.66	0.23	1.15	1.39	35.3	4.2	17.5
	70	**12.69**	**0.23**	**1.15**	**1.38**	**35.6**	**4.3**	**17.9**
	80	12.74	0.23	1.14	1.38	35.8	4.3	18.7

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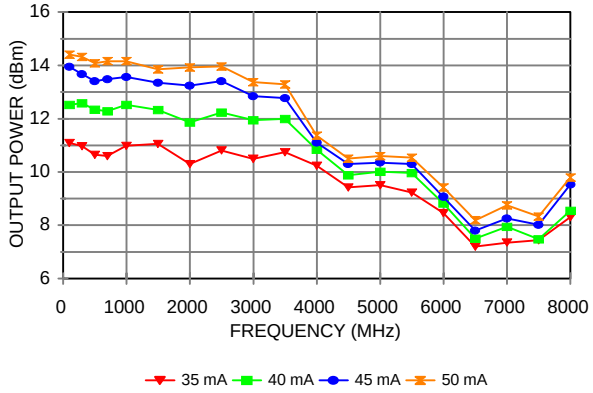
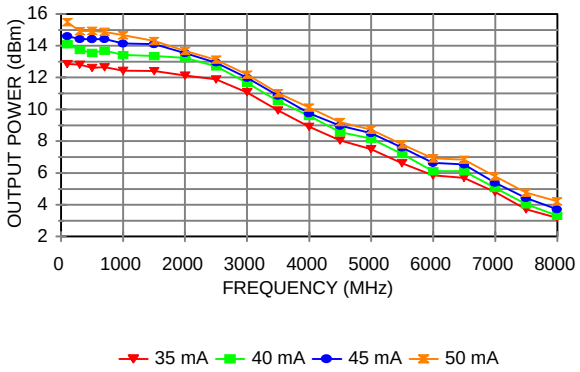
POUT VS.CURRENT

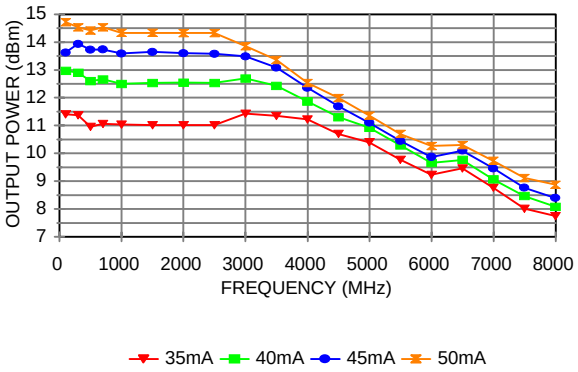
ERA-1 1dB COMPRESSION
At 35,40,45,50 mA Bias Currents



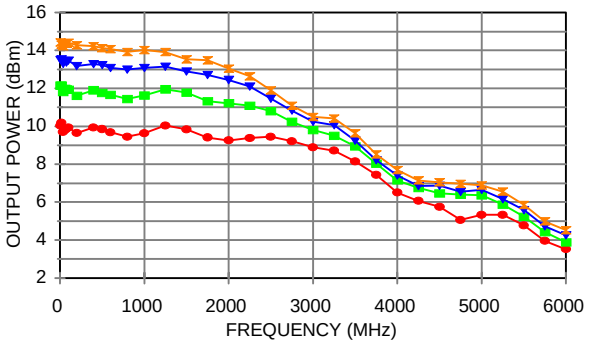
ERA-2 1dB COMPRESSION
At 35,40,45,50 mA Bias Currents



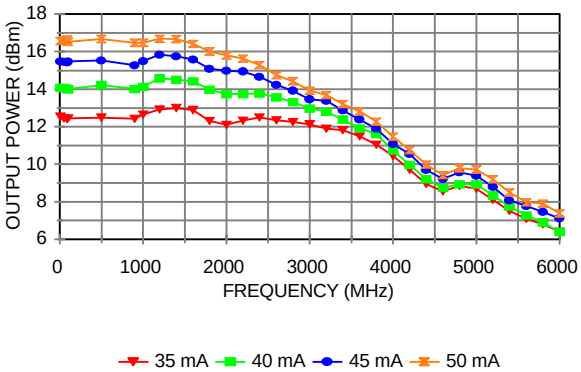
ERA-21 1dB COMPRESSION
At 35,40,45,50 mA Bias Currents



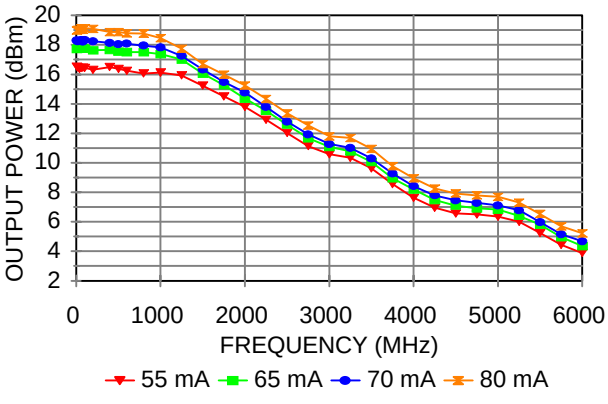
ERA-3 1dB COMPRESSION
At 25,30,35,40 mA Bias Currents



ERA-33 1dB COMPRESSION
At 35,40,45,50 mA Bias Currents



ERA-4 1dB COMPRESSION
At 55,65,70,80 mA Bias Currents



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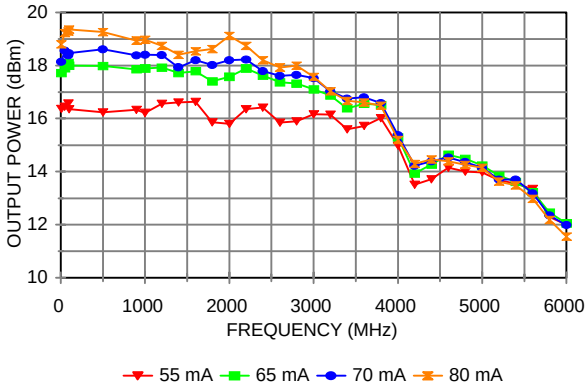
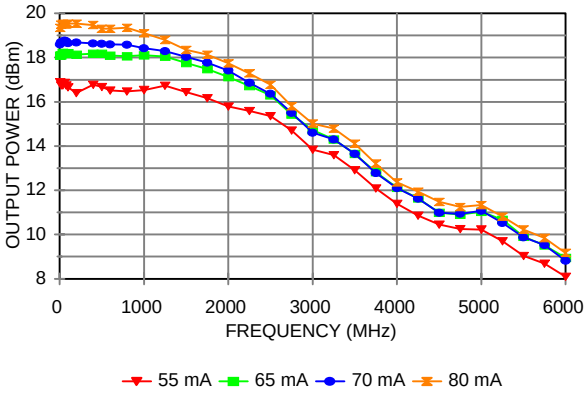
POUT VS.CURRENT

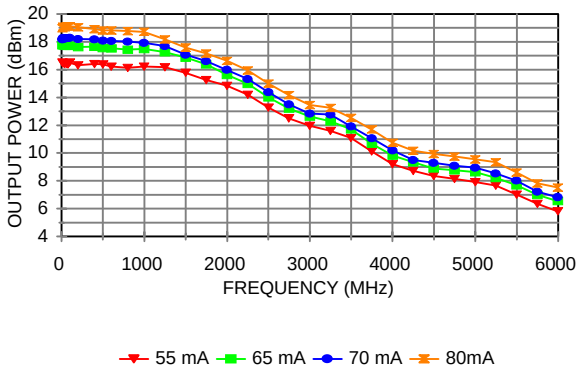
ERA-50 1dB COMPRESSION
At 55,65,70,80 mA Bias Currents



ERA-51 1dB COMPRESSION
At 55,65,70,80 mA Bias Currents



ERA-6 1dB COMPRESSION
At 55,65,70,80 mA Bias Currents



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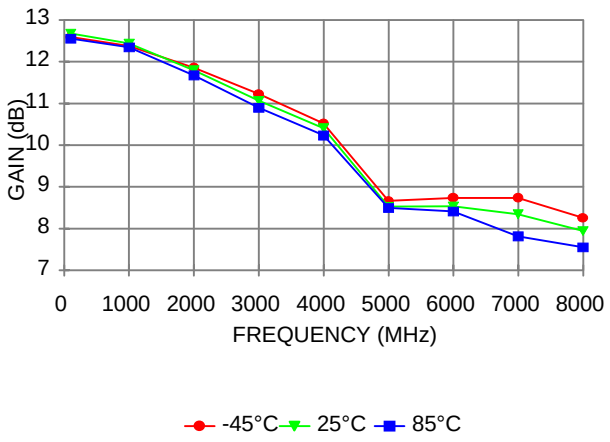
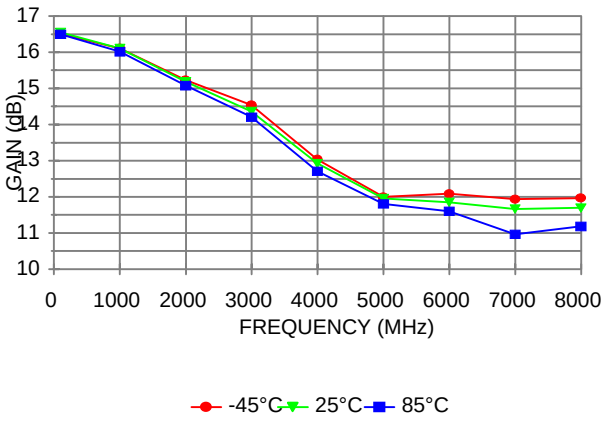
GAIN VS. TEMPERATURE

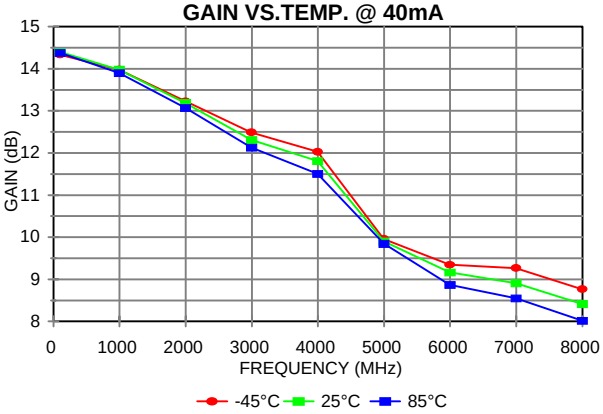
ERA-1
GAIN VS.TEMP @ 40 mA



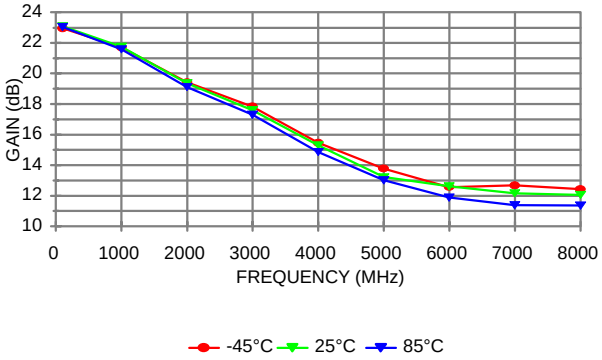
ERA-2
GAIN VS.TEMP. @ 40 mA



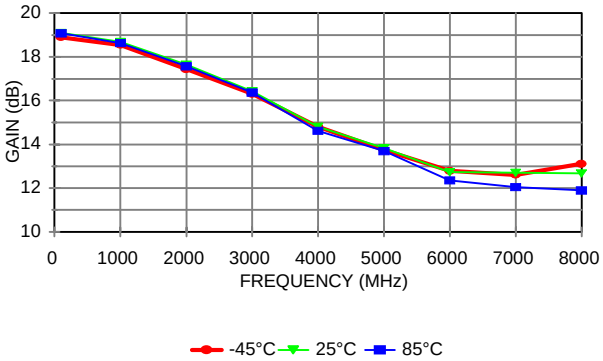
ERA-21
GAIN VS.TEMP. @ 40mA



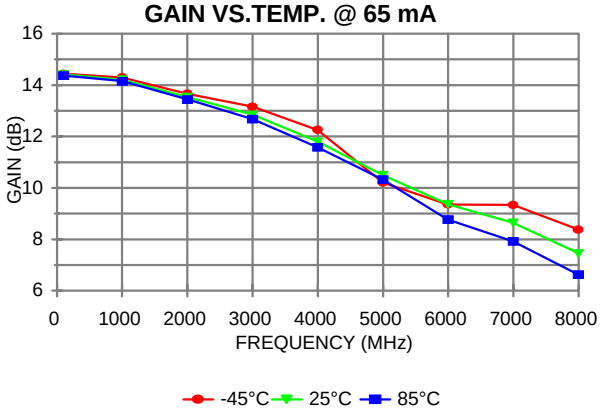
ERA-3
GAIN VS.TEMP. @ 35 mA



ERA-33
GAIN VS. TEMP @ 40 mA



ERA-4
GAIN VS.TEMP. @ 65 mA



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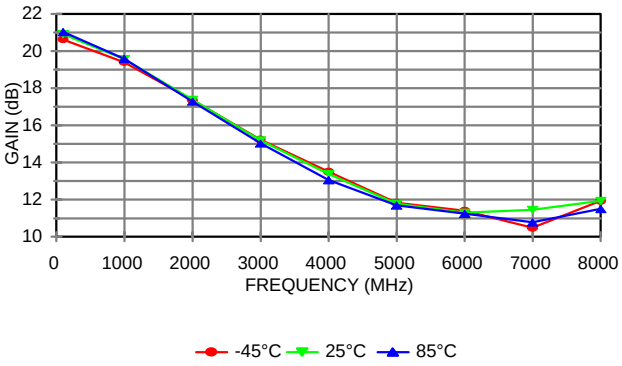
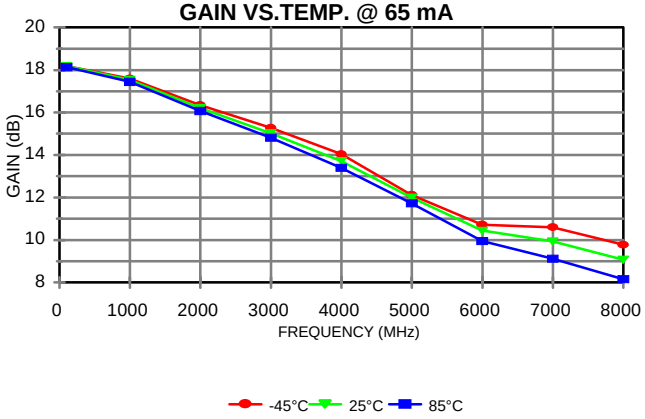
GAIN VS. TEMPERATURE

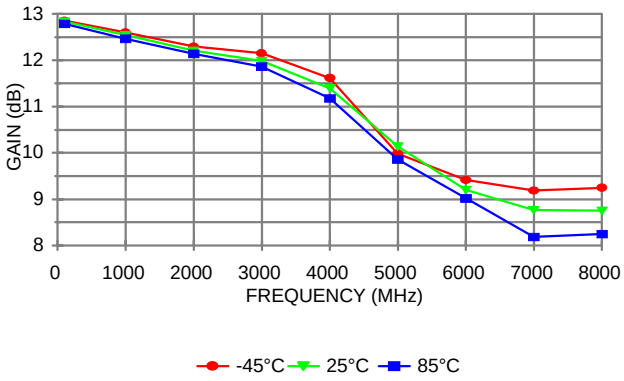
ERA-50
GAIN VS.TEMP @ 65 mA



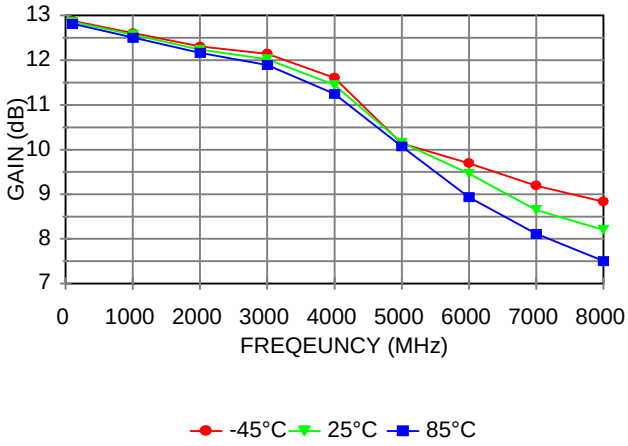
ERA-51
GAIN VS.TEMP. @ 65 mA



ERA-6
GAIN VS.TEMP @ 65 mA



ERA-6
GAIN VS. TEMP. @ 70 mA



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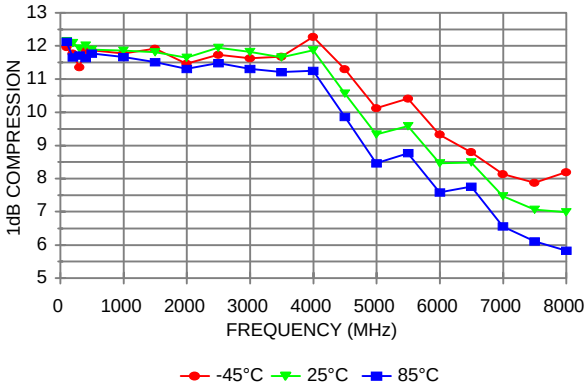
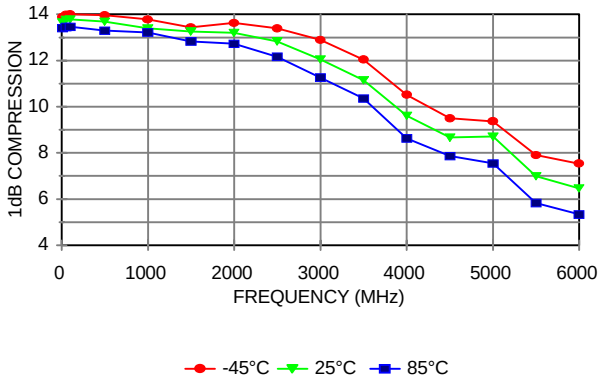
POUT VS. TEMPERATURE

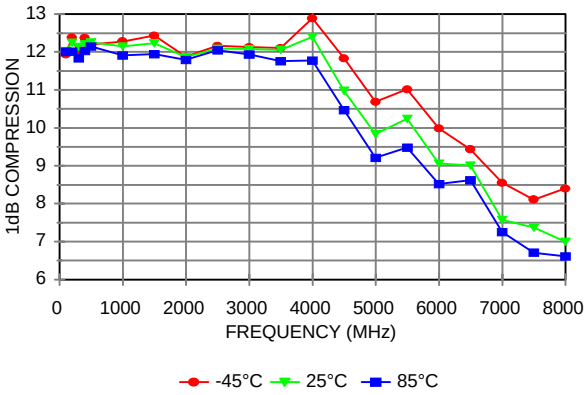
ERA-1
OUTPUT POWER VS. TEMPERATURE



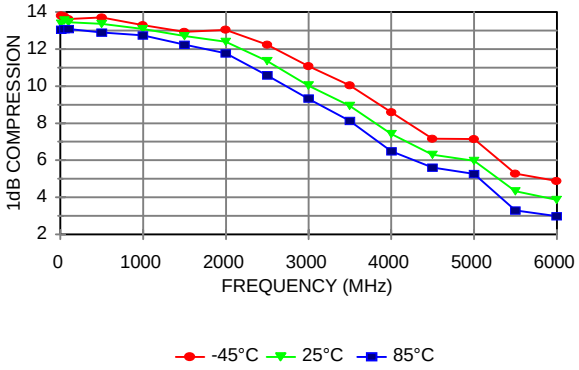
ERA-2
OUTPUT POWER VS.TEMPERATURE



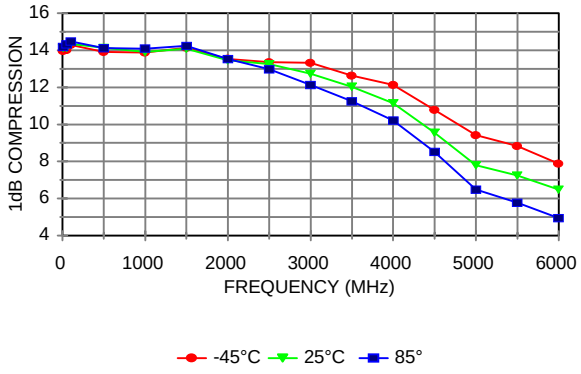
ERA-21
OUTPUT POWER VS. TEMPERATURE



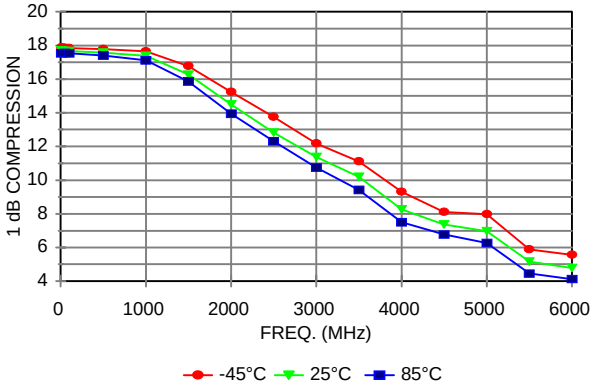
ERA-3
OUTPUT POWER VS.TEMPERATURE



ERA-33
OUTPUT POWER VS.TEMPERATURE



ERA-4
OUTPUT POWER VS. TEMPERATURE



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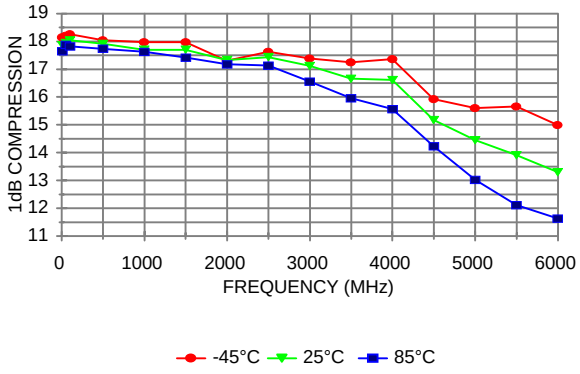
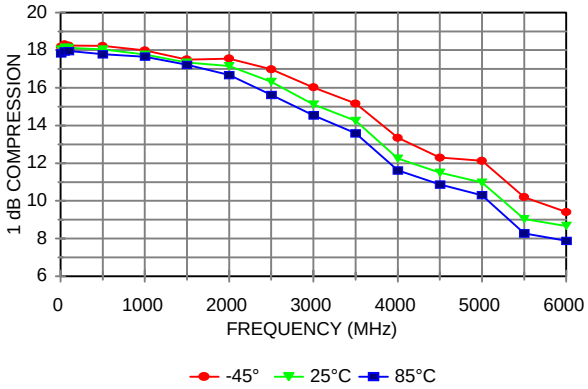
POUT VS. TEMPERATURE

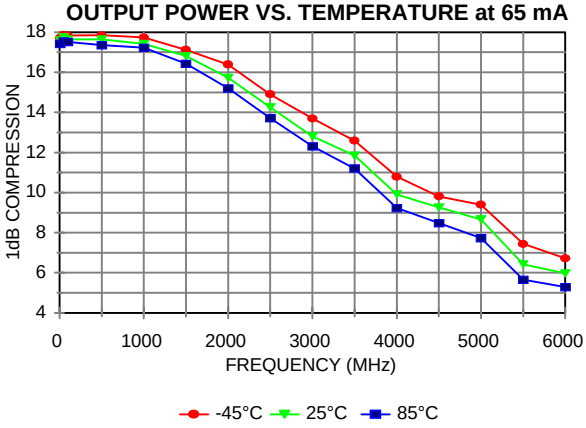
ERA-50
OUTPUT POWER VS.TEMPERATURE



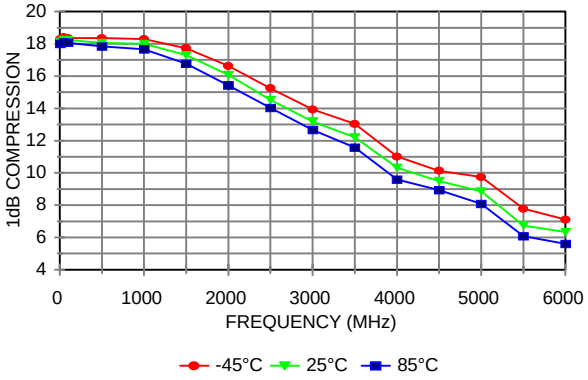
ERA-51
OUTPUT POWER VS. TEMPERATURE



ERA-6
OUTPUT POWER VS. TEMPERATURE at 65 mA



ERA-6
OUTPUT POWER VS.TEMPERATURE at 70 mA



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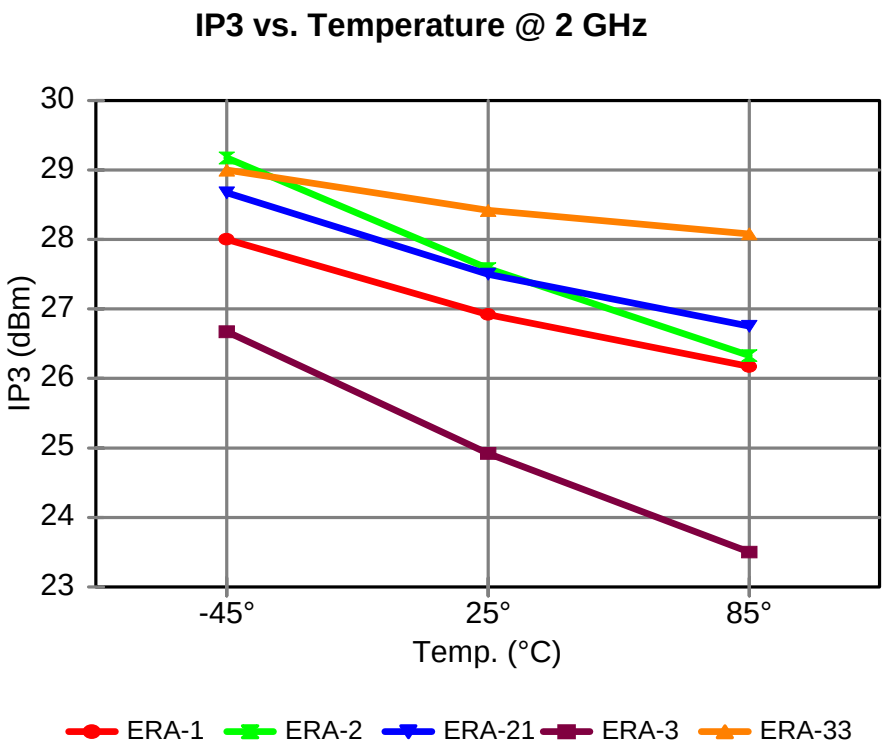
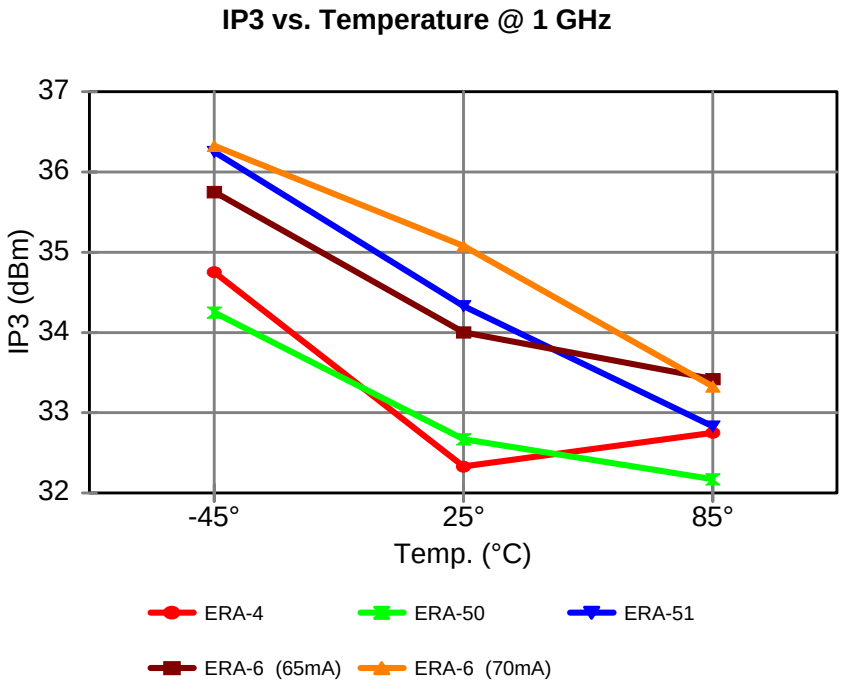
IP3 VS. TEMPERATURE





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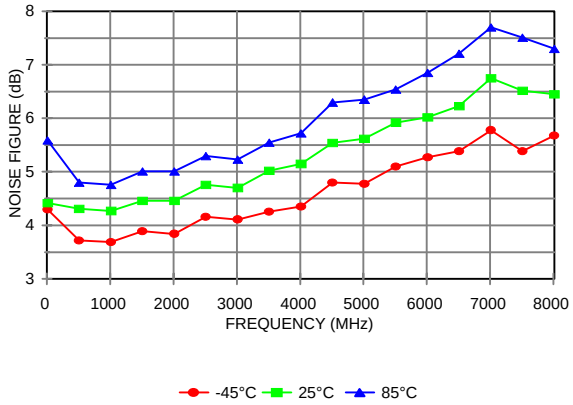
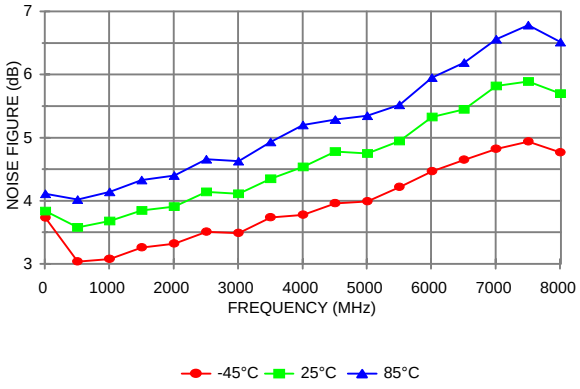
NOISE VS. TEMPERATURE

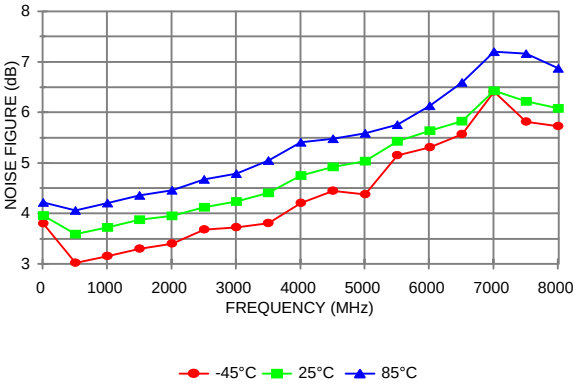
ERA-1
NOISE FIGURE



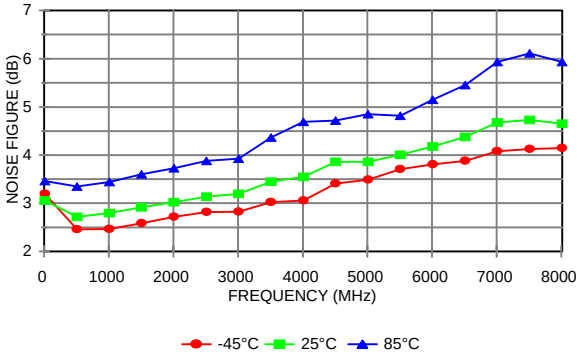
ERA-2
NOISE FIGURE



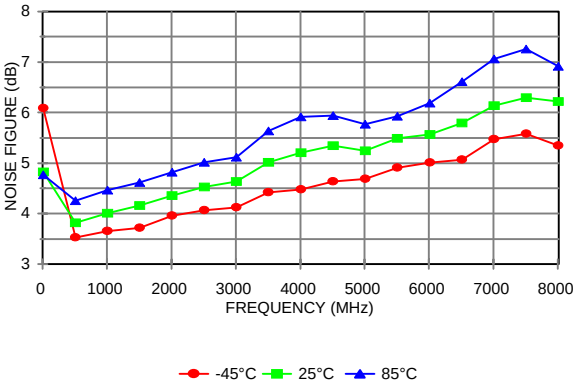
ERA-21
NOISE FIGURE



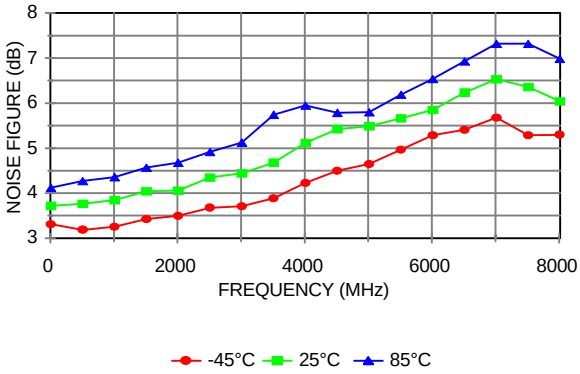
ERA-3
NOISE FIGURE



ERA-33
NOISE FIGURE



ERA-4
NOISE FIGURE



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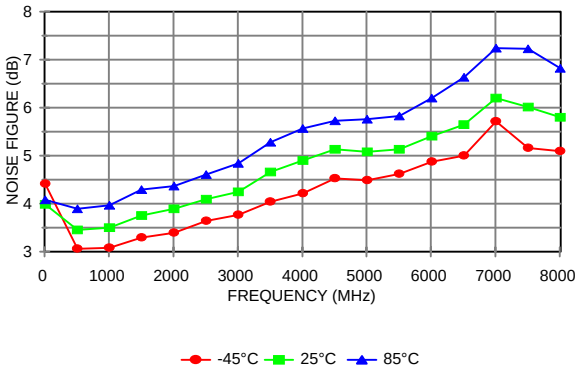
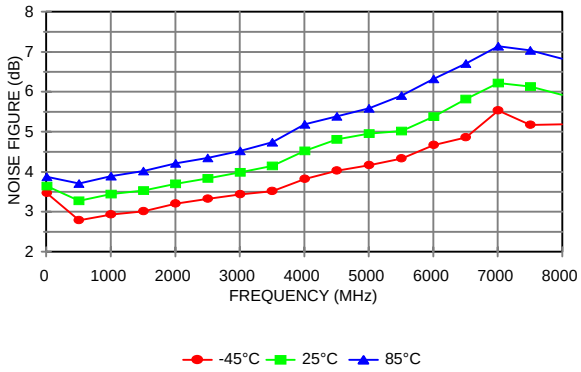
NOISE VS. TEMPERATURE

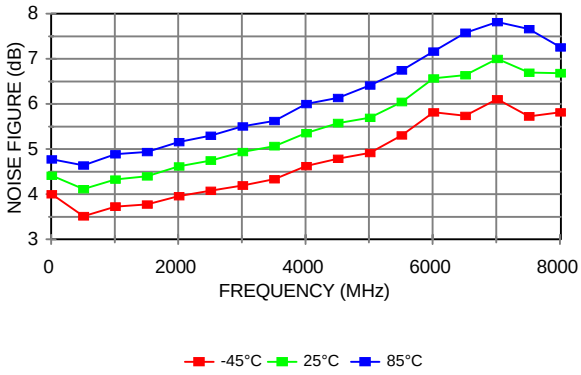
ERA-50
NOISE FIGURE



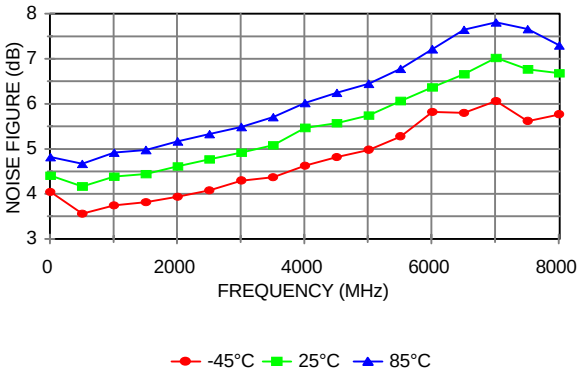
ERA-51
NOISE FIGURE



ERA-6
NOISE FIGURE



ERA-6 at 70 mA
NOISE FIGURE



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